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B028313(028)

B.Tech. (Third Semester) Examination

Nov.-Dec. 2020

(New Scheme)

DIGITAL SYSTEM DESIGN

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Attempt all questions. Part (a) is compulsory & Solve any two parts from (b), (c) and (d) of each questions.

Unit-I

1. (a) Write the Distributive Laws. 2

(b) Using Boolean Algebra, prove that : 7

(i) $AB + ABC + A\bar{B} = A$

(ii) $(B+A)(B+D)(A+C)(C+D) = BC + AD$

(iii) $AB + A'C = (A+C)(A'+B)$

(c) Reduce using mapping the following Boolean function in : 7

(i) Sum of products

(ii) Product of sums

Also implement it using Universal Gates

$F(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$

(d) Reduce the following expression using tabular method. 7

$F(A, B, C, D) = \sum m(0, 2, 3, 5, 8, 10, 11, 13)$

Unit-II

2. (a) Differentiate between combinational and sequential circuits. 2

(b) Design a Full adder circuit using Decoder. 7

(c) Draw the neat & clean diagram of BCD Adder and explain its working through table. 7

(d) What is Multiplexer? Write down its application and draw 16 : 1 multiplexer using only 2 : 1 multiplexer. 7

Unit-III

3. (a) Write difference between Latch and flip-flop. 2

(b) Draw the logic diagram of J-K flip-flop and explain its working to : 7

(i) Obtain the flip-flop characteristics table

(ii) Obtain characristics equation

(iii) Obtain excitation table

(c) Design BCD Ripple Counter and explain its functioning. 7

(d) What is Shift Register? Explain various types of shift register in brief. 7

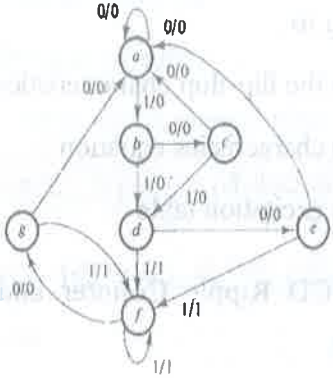
Unit-IV

4. (a) Compare Moore & Mealy FSM. 2

(b) What is Algorithmic State Machines charts? List the silent features of the ASM charts. 7

(c) Design a Pulse train generator using a shift register to generate the following waveform : 7

(d) Reduce the number of states in the following state table and tabulate the reduced state table and also draw the reduced state diagram. 7



Unit-V

5. (a) Define Fan-in and Fan-out. 2

(b) Give comparison among various logic families. 7

(c) Draw the circuit diagram and explain the operation of 2 inputs TTL NAND gate with totem - pole output. 7

(d) Draw two input CMOS NAND & NOR gate and explain their operations. 7